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--1. (Amended) A method comprising:

compressing a plurality of pixel values and a rounding vector into a first sum vector and a first carry vector;

discarding a least significant bit of the first carry vector;

discarding a two least significant bits of the first sum vector; and

adding the first sum vector and the first carry vector to generate a pixel average value.

2. The method of claim 1, wherein said adding the first sum vector and the first carry vector is performed with a Single-Instruction/Multiple-Data (SIMD) adder.

3. The method of claim 1, wherein said compressing a plurality of pixel values and a rounding vector comprises compressing four pixel values and a rounding vector.

4. The method of claim 3, wherein the pixel values comprise 8-bit values.

5. The method of claim 4, wherein the 8IND adder comprises a 36-bit adder including one dummy bit for each of four byte locations.

6. The method of claim 1, wherein the rounding vector is 10_2.

7. The method of claim 3, wherein said compressing four pixel values and a rounding vector is performed in three stages.

8. The method of claim 7, wherein said three stages comprise:

compressing three of said four pixel values into a second sum vector and a second carry vector;

compressing the fourth pixel value, the rounding vector, and the second sum vector into a third sum vector and a third carry vector; and

compressing the second carry vector, third sum vector and third carry vectors into said first sum and first carry vectors.

9. (Amended) Apparatus comprising:

a compressor stage including a plurality of compressors, each compressor operative to compress a plurality of operands and a rounding vector into a first sum vector and a first carry vector and to discard a two least significant bits (LSBs) of said first sum vector and an LSB of the first carry vector; and

a Single-Instruction/Multiple-Data (SIMD) adder operative to add the first sum vector and the first carry vector to generate an average pixel value.

10. The apparatus of claim 9, wherein said plurality of compressors comprises four compressors.

11. The apparatus of claim 9, wherein each compressor is operative to compress four operands and a rounding vector.

12. The apparatus of claim 9, wherein said pixel values and the average pixel value comprise 8-bit values.

13. The apparatus of claim 12, wherein the SIMD adder includes one dummy bit per byte location.

14. The apparatus of claim 8, wherein the rounding vector is 10₂.

15. The apparatus of claim 11, wherein each compressor comprises:

a first compressor operative to compress three of said four pixel values into a second sum vector and a second carry vector;

a second compressor operative to compress the fourth pixel value, the rounding vector, and the second sum vector into a third sum vector and a third carry vector; and

a third compressor operative to compress the second carry vector, third sum vector and third carry vectors into said first sum and first carry vectors.

16. (Amended) An article comprising a machine-readable medium include machine readable instructions, the instructions operative to cause a machine to:

compress a plurality of pixel values and a rounding vector into a first sum vector and a first carry vector;

discard a least significant bit of the first carry vector;

discard a two least significant bits of the first sum vector; and

add the first sum vector and the first carry vector to generate a pixel average value.--

17. The article of claim 16, adding the first sum vector and the first carry vector is performed with a Single-Instruction/Multiple-Data (SIMD) adder.

18. The article of claim 16, wherein the instructions for compressing a plurality of pixel values and a rounding vector comprise instructions operative to cause the machine to compress four pixel values and a rounding vector.

19. The article of claim 18, wherein the pixel values comprise 8-bit values.

20. The article of claim 19, wherein the SIMD adder comprises a 36-bit adder including one dummy bit for each of four byte locations.

21. The article of claim 16, wherein the rounding vector is 10_2.

22. The article of claim 18, wherein the instructions causing the machine to compress four pixel values and a rounding vector comprise instructions causing the machine to compress the vectors in three stages.

23. The article of claim 22, wherein instructions causing the machine to compress the vectors in three stages comprising instructions causing the machine to:

compress three of said four pixel values into a second sum vector and a second carry vector;

compress the fourth pixel value, the rounding vector, and the second sum vector into a third sum vector and a third carry vector; and

compress the second carry vector, third sum vector and third carry vectors into said first sum and first carry vectors.